K24C64

I²C-Compatible Serial E²PROM

Data Sheet Rev. 1.1

General Description

The K24C64 is a 64-Kbit I²C-compatible Serial EEPROM (Electrically Erasable Programmable Memory) device. It contains a memory array of 8K × 8 bits, which is organized in 32-byte per page. K24C64 provides the following devices for different application.

Device Selection Table

Device Name	Voltage Range	Temp. Range	Max. Clock Frequency
K24C64-MI	1.7V~5.5V	-40°C ~ 85°C	1MHz[1]
K24C64-NK	1.8V~5.5V	-40°C~105°C	1MHz[1]
K24C64-DE	2.5V~5.5V	-40°C~125°C	1MHz

Note 1: 400 kHz for V_{CC} < 2.5V.

Features

- Single Supply Voltage and High Speed
  - Minimum operating voltage down to 1.7V
  - 1 MHz clock from 2.5V to 5.5V
  - 400kHz clock from 1.7V to 2.5V
- Low power CMOS technology
  - Read current 400uA, maximum
  - Write current 1.0mA, maximum
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Sequential & Random Read Features
- 32 byte Page Write Modes, Partial Page Writes Allowed
- Write protect of the whole memory array
- Additional Write Lockable Page
- Self-timed Write Cycle (5ms maximum)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - HBM: 6KV
  - Latch up Capability: +/- 200mA (25°C & 125°C)

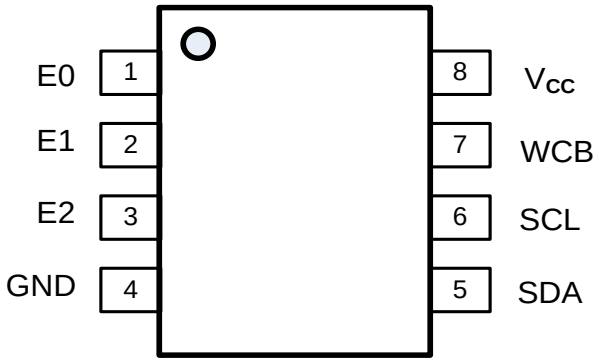
Package

- 8-Pin PDIP
- 8-Pin SOP
- 8-Pin TSSOP
- 8-Pin DFN

1. Pin Configuration

1.1 Pin Configuration

Figure 1-1 Pin Configuration



1.2 Pin Definition

Table 1-1 Pin Definition

Pin	Name	Type	Description
1	E0	I/O	Slave Address Setting
2	E1	Input	Slave Address Setting
3	E2	Input	Slave Address Setting
4	GND	Ground	Ground
5	SDA	I/O	Serial Data Input and Serial Data Output
6	SCL	Input	Serial Clock Input
7	WCB	Input	Write Control, Low Enable Write
8	V_{cc}	Power	Power