High-PSRR Low-Noise RF LDO HL57XX Series

CMOS Voltage Regulator With ON/OFF Switch 300mA

The HL57XX series is a low-noise LDO that can supply up to 300 mA output current. Designed to meet the requirements of RF and analog circuits, the HL57XX series device provides low noise, high PSRR, low quiescent current, and low line or load transient response figures. Using new innovative design techniques, the HL57XX series offers ultra-low noise performance without a noise bypass capacitor and the ability for remote output capacitor placement**.** response figures with a 1-µF input and a 1-µF output ceramic capacitor

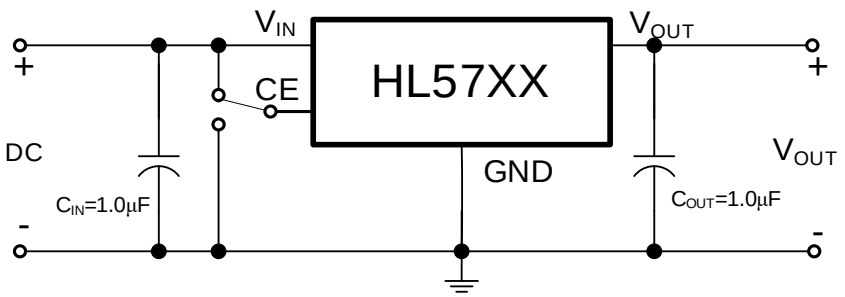
■ Features:

- Input Voltage Range: 2.2 V to 5.5 V
- Output Voltage Range: 1.2 V to 4.5 V
- Stable With 1-µF Ceramic Input and Output Capacitors
- No Noise Bypass Capacitor Required
- Remote Output Capacitor Placement
- Current Limiter and Over Temperature Protection
- -40°C to 125°C Operating Junction Temperature
- Low Output Voltage Noise: 20µV_{RMS}
- High PSRR: 90dB@1kHz
- Output Voltage Tolerance: ±1%
- Low quiescent Current: 20uA
- Low Dropout Voltage: 120mV@300mA

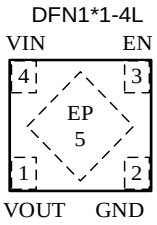
■ Applications:

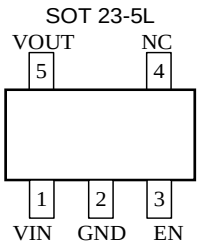
- Mobile Phones, Tablets
- Digital Cameras and Audio Devices
- Portable and Battery-Powered Equipment
- Portable Medical Equipment
- Smart Meters and Field Transmitters
- RF, PLL, VCO, and Clock Power Supplies
- IP Cameras
- Drones

■ Typical Application:



■ Pin Configuration (Top View):





■ Product Selections:

Product Name	V_{OUT} (V)	Package	Ordering Name	Marking	Package Information
HL5712	1.2	DFN1*1-4L	HL57E12WB6	5712	Tape and Reel, 10000pcs
HL5715	1.5	DFN1*1-4L	HL57E15WB6	5715	
HL5718	1.8	DFN1*1-4L	HL57E18WB6	5718	
HL5721	2.1	DFN1*1-4L	HL57E21WB6	5721	
HL5725	2.5	DFN1*1-4L	HL57E25WB6	5725	
HL5728	2.8	DFN1*1-4L	HL57E28WB6	5728	
HL5730	3.0	DFN1*1-4L	HL57E30WB6	5730	
HL5733	3.3	DFN1*1-4L	HL57E33WB6	5733	
HL5736	3.6	DFN1*1-4L	HL57E36WB6	5736	
HL5712	1.2	SOT23-5L	HL57E12QC3	5712	Tape and Reel, 3000pcs
HL5715	1.5	SOT23-5L	HL57E15QC3	5715	
HL5718	1.8	SOT23-5L	HL57E18QC3	5718	
HL5721	2.1	SOT23-5L	HL57E21QC3	5721	
HL5725	2.5	SOT23-5L	HL57E25QC3	5725	
HL5728	2.8	SOT23-5L	HL57E28QC3	5728	
HL5730	3.0	SOT23-5L	HL57E30QC3	5730	
HL5733	3.3	SOT23-5L	HL57E33QC3	5733	
HL5736	3.6	SOT23-5L	HL57E36QC3	5736	
HL5745	4.5	SOT23-5L	HL57E47QC3	5747	

Notes:

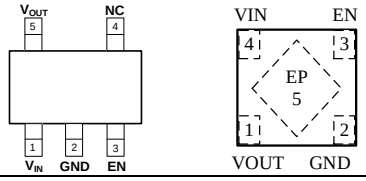
1* Customer can request to customize the output voltage ranged from 1.2V to 4. 5V if desired voltage is not found in the selections.

2* Customer can request customization of package choice.

3* Please pay attention to the MARKING of the product package type.

■ Ordering Information

HL57 ①②③④⑤⑥⑦ e.g. HL57E33QC3

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	PIN Configuration	E	
②③	Output Voltage	18~	e.g. 1.8V→②=1, ③=8
④	Packages Type	Q	SOT23
		W	DFN
⑤	Packages Count	A~Z	e.g. A=3, B=4, C=5 ~
⑥	Minimum Packing Quantity	0~6	0=100, 1=1000, 2=2500, 3=3000, 4=4000, 5=5000, 6=10000
⑦	Customer can request customization of product		

■ Absolute Maximum Ratings:

(Unless otherwise indicated**:** T_a=25℃**)**

PARAMETER	SYMBOL	RATINGS		UNITS
Input Voltage	V_{IN}	-0.3 ~ 6.0		V
Output Voltage	V_{OUT}	-0.3 ~ V_{IN}+0.3V		
Power Dissipation	P_D	SOT23-5L	250	mW
		DFN1*1-4L	200	
Thermal Resistance	$R_{\theta JB}$ (1)	SOT23-5L	180	℃/W
		DFN1*1-4L	160	
Operating Ambient Temperature	T_{opr}	-40 ~ +85		℃
Storage Temperature	T_{stg}	-40 ~ +125		
ESD Protection	ESD HBM	6000		V

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

(1) Mounted on JEDEC standard 4layer (2s2p) PCB test board

■ Notes on Use:

Input Capacitor (C_{IN}): 1.0μF above

Output Capacitor (C_{OUT}):1.0μF above

■ Electrical Characteristics:

HL57XX Series (Unless otherwise indicated：T_a=25℃)

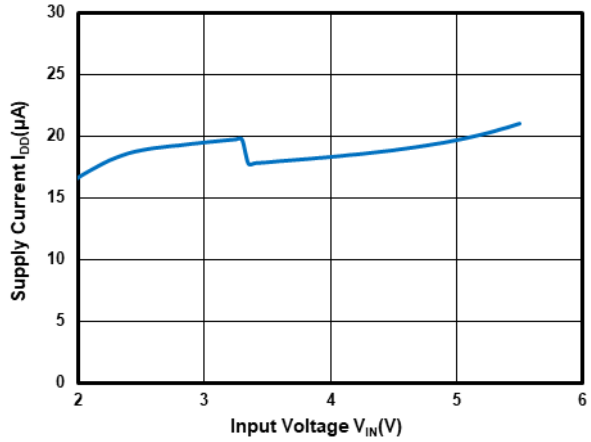
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	$V_{OUT(S)}$	$V_{IN}=V_{OUT(S)}+2.0V$ I_{OUT}=1mA, $V_{OUT(S)}$＜2.0V	$V_{OUT(S)}$-0.03	$V_{OUT(S)}$	$V_{OUT(S)}$+0.03	V
		$V_{IN}=V_{OUT(S)}+1.0V$ I_{OUT}=1mA, $V_{OUT(S)}$≥2.0V	$V_{OUT(S)}$×0.98		$V_{OUT(S)}$×1.02	
Dropout Voltage*1	V_{DROP}	$V_{EN}=V_{IN}$, V_{OUT}＜3V I_{OUT}=300mA		130		mV
		$V_{EN}=V_{IN}$, V_{OUT}≥3V I_{OUT}=300mA		120		
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN} \bullet V_{OUT(s)}}$	$V_{OUT(S)}+1.0V \le V_{IN}=V_{EN} \le 5.5V$ I_{OUT}=10mA		0.02	0.1	%/V
Line Transient	ΔV_{OUT_Line}	$V_{IN}=V_{OUT}+1V$ to $V_{OUT}+2V$ in 30us	-1			mV
		$V_{IN}=V_{OUT}+2V$ to $V_{OUT}+1V$ in 30us			1	
Load Regulation	ΔV_{OUT2}	$V_{IN}=V_{EN}=V_{OUT(S)}+1.0V$ 1mA≤I_{OUT}≤300mA		10	20	mV
Load Transient	ΔV_{OUT_Load}	I_{OUT}=1mA to 300mA in 10μs	-40			mV
		I_{OUT}=300mA to 1mA in 10μs			40	
Temperature Stability	$\frac{\Delta V_{OUT}}{\Delta T_a \bullet V_{OUT(s)}}$	$V_{IN}=V_{EN}=V_{OUT(S)}+1.0V$ I_{OUT}=1mA , -40℃≤T_a≤125℃		±100		ppm/℃
GND Current ($V_{EN}=V_{IN}$)	I_{GND}	no load		20	40	μA
		I_{OUT}=300mA		470		μA
Shutdown Current	I_{SHUT}	V_{IN}=5.5V, V_{EN}=0		0.01	0.1	μA
Input Voltage	V_{IN}	---	2.2		5.5	V
Maximum Output Current	I_{OUTMAX}		250	300		mA
Current Limit*2	I_{LIM}	$V_{IN}=V_{EN}=V_{OUT(S)}+1.0V$ V_{OUT} = 0.95 ×$V_{OUT(S)}$		500		mA
C_{OUT} Auto Discharge	R_{DCHG}	V_{EN}=0, $V_{OUT}=V_{OUT(S)}$		240		Ω
Power Supply Rejection Ratio	PSRR	f=1kHz, I_{OUT}=20mA		94		dB
		f=10kHz, I_{OUT}=20mA		72		
		f=100kHz, I_{OUT}=20mA		77		
		f=1MHz, I_{OUT}=20mA		53		
Output noise voltage	e_N	I_{OUT}=20mA		20		μV_{RMS}
Start-Up Time	T_{START}	From $V_{EN}>V_{ENH}$ to V_{OUT}=95% of V_{OUT}		80	150	μs
Overshoot on Start-Up	$\Delta V_{OUT\_Start-up}$	Stated as a percentage of $V_{OUT(S)}$			5	%
EN 'H' Level Voltage	V_{ENH}	---	0.85		5.5	V
EN 'L' Level Voltage	V_{ENL}	---	0		0.35	
EN 'H' Level Current	I_{ENH}	V_{IN}=5.5V, V_{EN} =V_{IN}	-0.1		0.1	μA
EN 'L' Level Current	I_{ENL}	V_{IN}=5.5V, V_{EN} =0	-0.1		0.1	
Over Temperature Protection	OTP	I_{OUT}=1mA		155		℃

Notes：

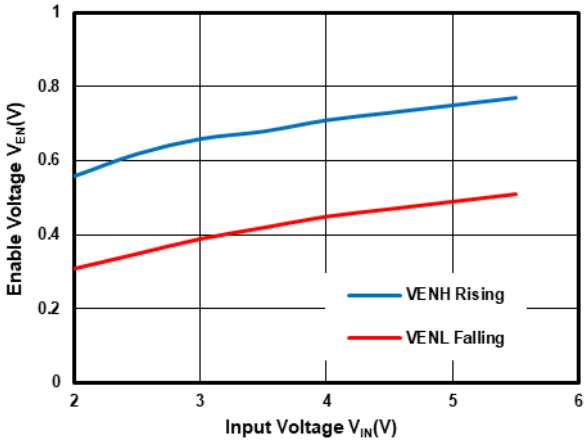
1. $V_{DROP}=V_{IN1}$ -（$V_{OUT(S)}$× 0.98）where V_{IN1} is the input voltage when V_{OUT} = $V_{OUT(S)}$× 0.98.
2. I_{LIM}: Output current when $V_{IN}=V_{OUT(S)}+1V$ and V_{OUT} = 0.95*$V_{OUT(S)}$.

■ Typical Performance Characteristics:

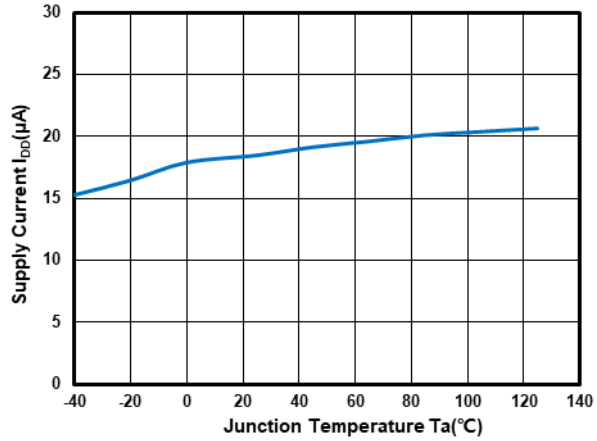
Test Conditions: V_{IN}=4.3V, V_{OUT}=3.3V, C_{IN}=1.0μF, C_{OUT}=1.0μF, T_a=25℃, unless otherwise indicated.



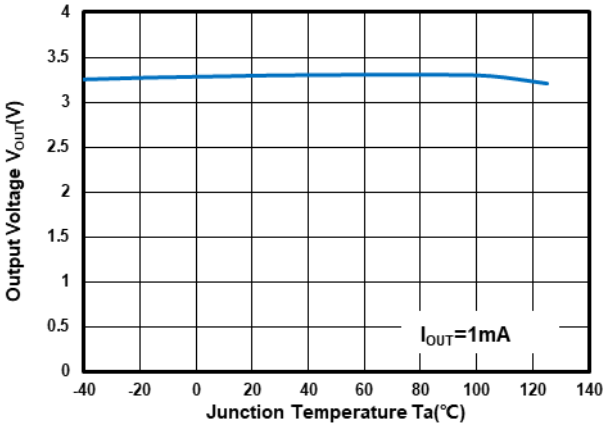
Supply Current vs. Input Voltage



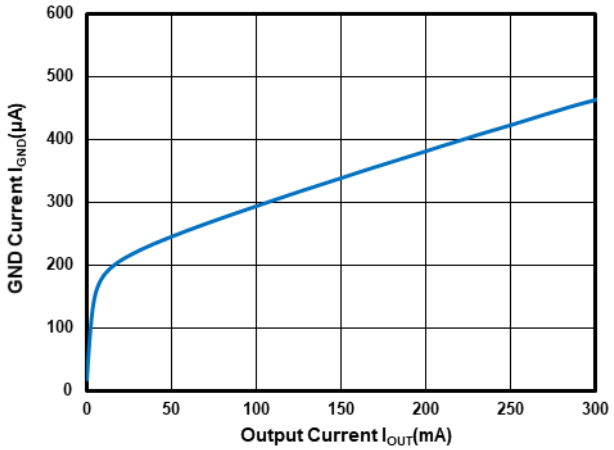
V_{EN} Thresholds vs. Input Voltage



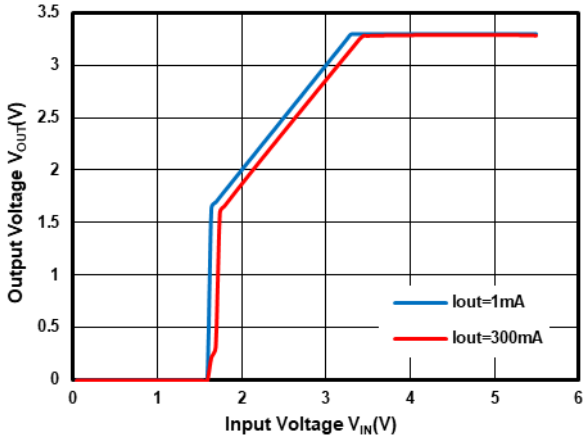
Supply Current vs. Temperature



Output Voltage vs. Temperature



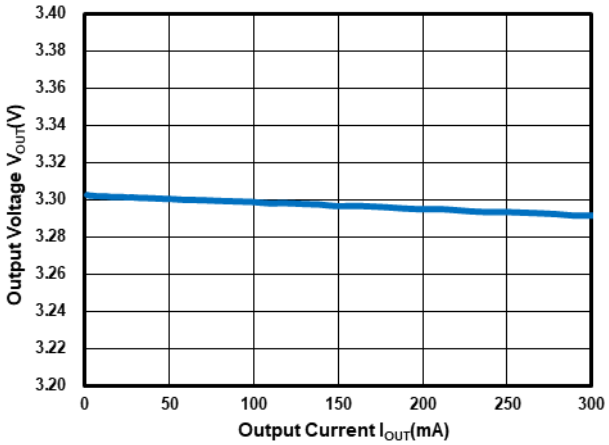
GND Current vs. Output Current



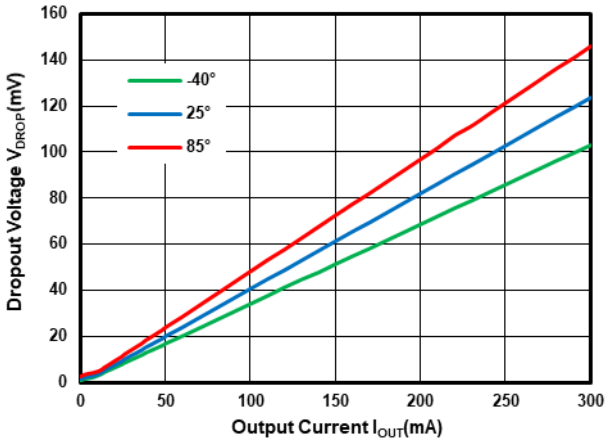
Output Voltage vs. Input Voltage

■ Typical Performance Characteristics (Continued):

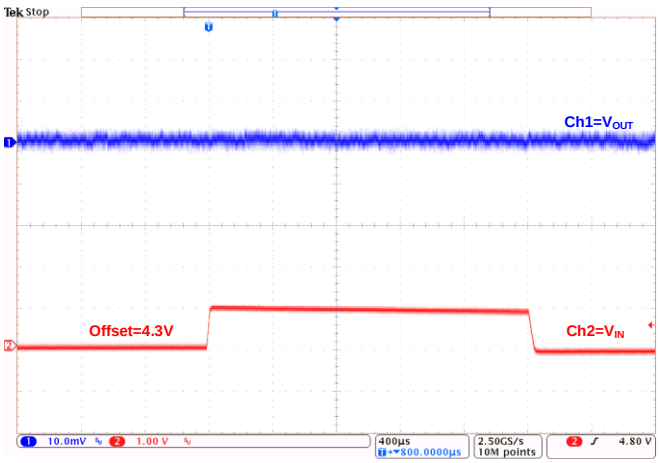
Test Conditions: V_{IN}=4.3V, V_{OUT}=3.3V, C_{IN}=1.0μF, C_{OUT}=1.0μF, T_a=25℃, unless otherwise indicated.



Output Voltage vs. Output Current

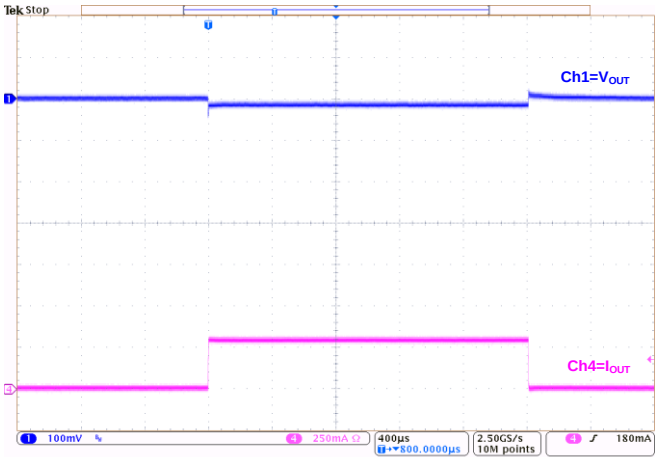


Dropout Voltage vs. Output Current



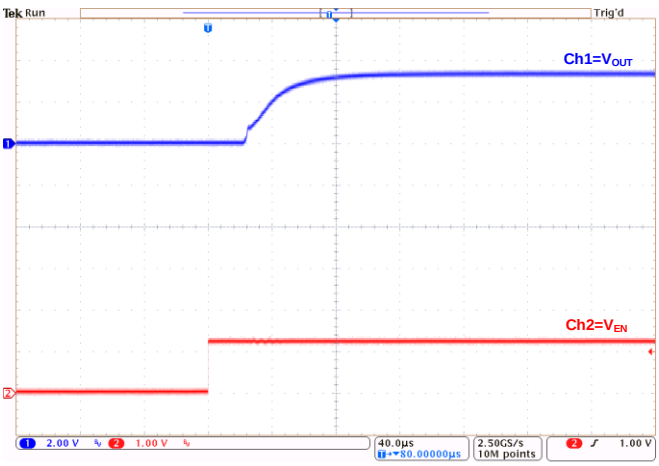
Line Transient:

(I_{OUT}=10mA)



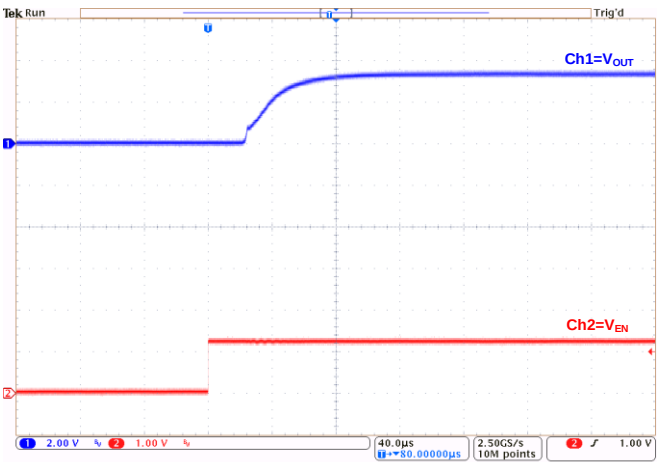
Load Transient:

(I_{OUT}=0mA~300mA~0mA)



EN Enable:

(I_{OUT}=0mA)

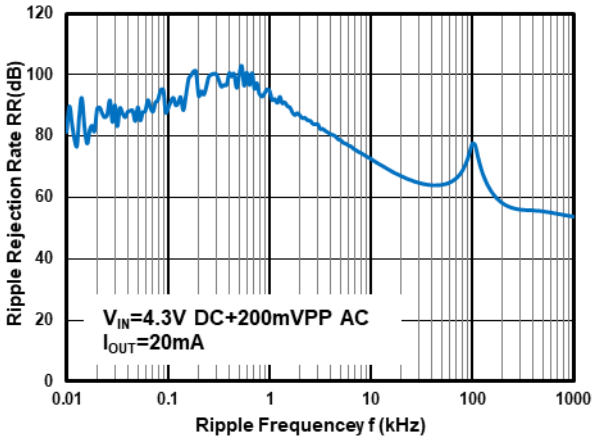


EN Enable:

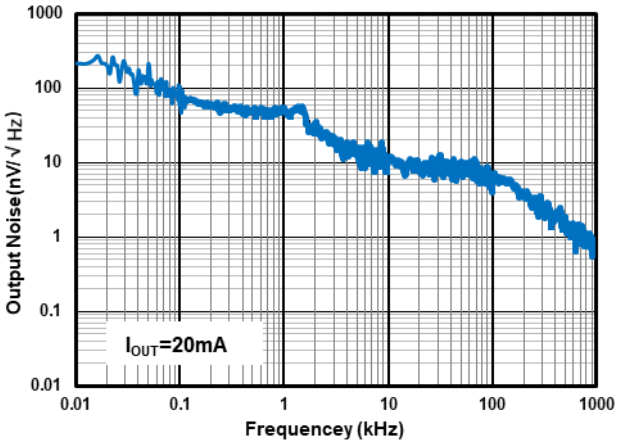
(I_{OUT}=300mA)

■ Typical Performance Characteristics (Continued):

Test Conditions: V_{IN}=4.3V, V_{OUT}=3.3V, C_{IN}=1.0μF, C_{OUT}=1.0μF, T_a=25℃, unless otherwise indicated.



Power Supply Rejection Ratio



Noise Density Test

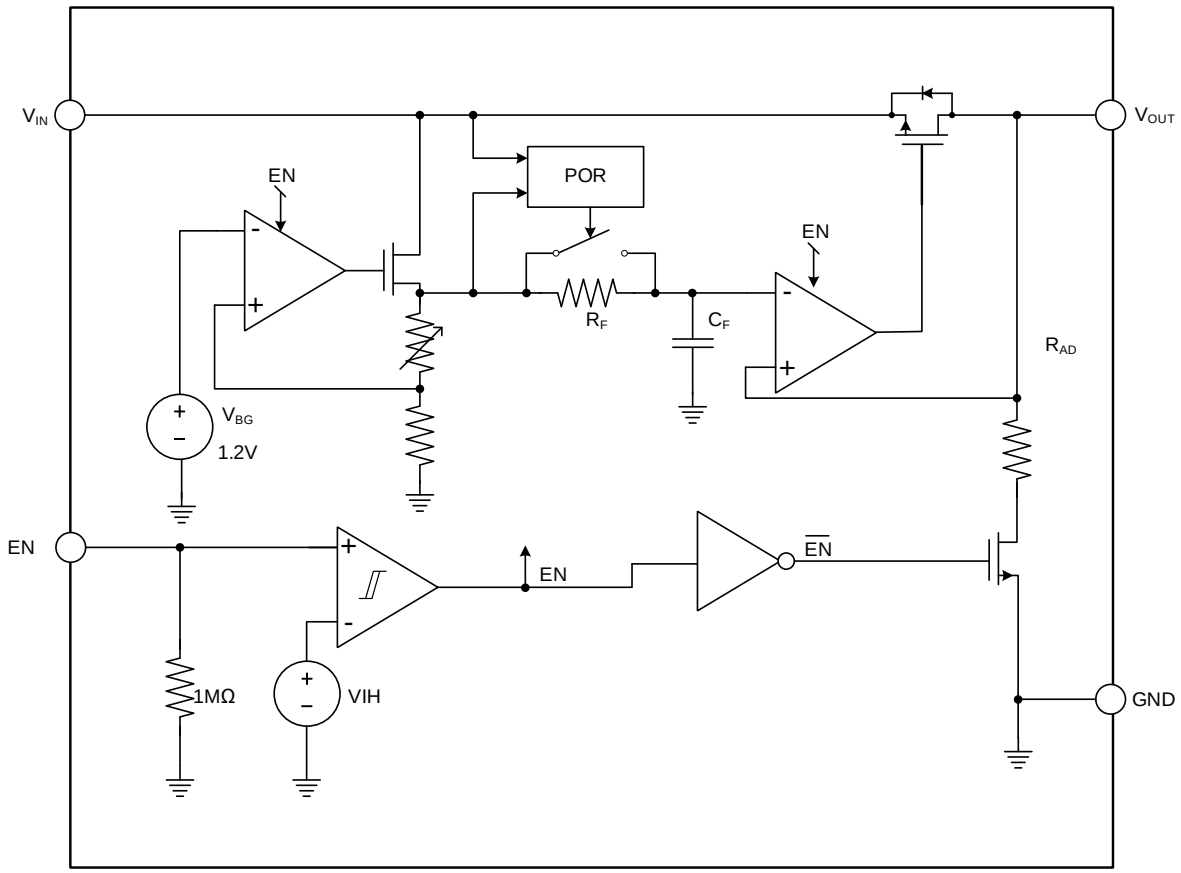
■ Detailed Description:

1. Overview

Using new innovative design techniques, the HL57XX series offers ultra-low noise performance without the need for a separate noise filter capacitor.

The HL57XX series is designed to perform with a single 1-μF input capacitor and a single 1-μF ceramic output capacitor. With a reasonable PCB layout, the single 1-μF ceramic output capacitor can be placed up to 10 cm away from the HL57XX series device.

2. Functional Block Diagram



■ Feature Description

1. Enable (EN)

The HL57XX series EN pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{ENH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{ENL} threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

2. Low Output Noise

Any internal noise at the HL57XX series reference voltage is reduced by a first order low-pass RC filter before it is passed to the output buffer stage. The low-pass RC filter has a –3 dB cut-off frequency of approximately 0.1 Hz.

3. Output Automatic Discharge

The HL57XX series output employs an internal 240-Ω (typical) pulldown resistance to discharge the output when the EN pin is low, and the device is disabled

4. Remote Output Capacitor Placement

The HL57XX series requires at least a 1-µF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10 cm away from the LDO.

5. Over Temperature Protection (OTP)

Over temperature protection disables the output when the junction temperature rises to approximately 160°C which allows the device to cool. When the junction temperature cools to approximately 135°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

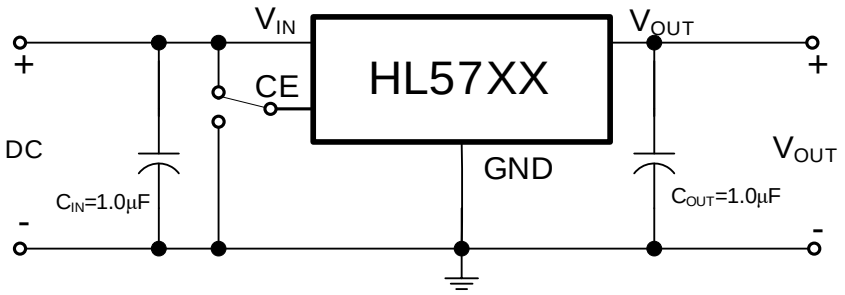
The over temperature protection circuitry of the HL57XX series has been designed to protect against temporary thermal overload conditions. The OTP circuitry was not intended to replace proper heat-sinking. Continuously running the HL57XX series device into thermal shutdown may degrade device reliability.

■ Application and Implementation

The HL57XX series is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 1 µF. The HL57XX series delivers this performance in industry standard packages such as SOT23-5, for this device, are specified with an operating junction temperature (T_J) of –40°C to 125°C.

1. Typical Application

As the figure shows the typical application circuit for the HL57XX series. Input and output capacitances may need to be increased above the 1 µF minimum for some applications.



2. Design Requirements

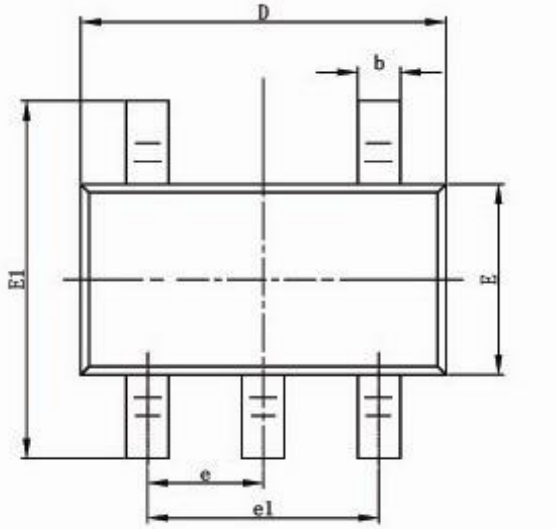
DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.2 V to 5.5 V
Output voltage	1.8 V
Output current	300 mA
Output capacitor range	1 µF to 10 µF
Input/Output capacitor ESR range	5 to 500 mΩ

Notes:

1. If the impedance of the power supply is high, which is caused by forgetting installing input capacitor or installing too small value capacitor, the oscillation may occur.
2. Pay attention to the operation conditions of input and output voltage and load current, such that the power consumption in the IC should not exceed the allowable power consumption of the package even though the chip has short circuit protection.
3. IC has a built-in anti-static protection (ESD) circuit, but please do not add excessive stress to the IC.

■ Packaging Information

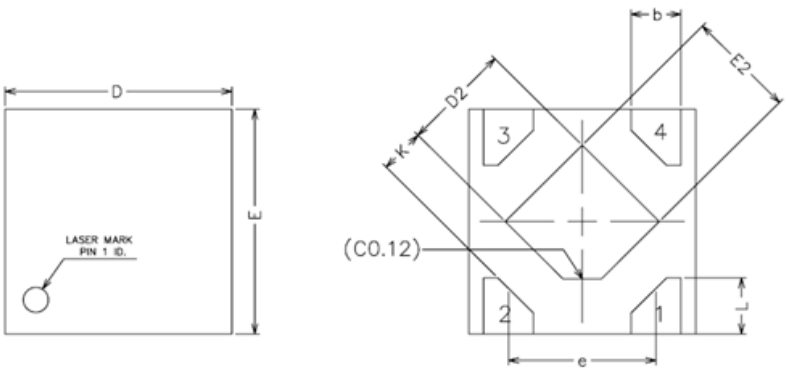
SOT-23-5L PACKAGE OUTLINE DIMENSIONS

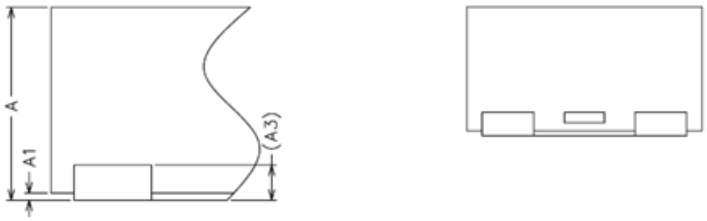


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

■ Packaging Information (Continued)

DFN(1*1)-4L PACKAGE OUTLINE DIMENSIONS





COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.100REF	
b	0.17	0.22	0.27
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
L	0.20	0.25	0.30
e	0.60	0.65	0.70
K	0.15	–	–

■ Revision History

Changes from Version V1.0 (December 2020) to Version V1.1

- Change I_{GND} max of no load from 30uA to 40uA in Electrical Characteristics table……...4